REMARKS

Claims 1-19 are pending in the application. By this amendment, claim 6 is being amended to overcome the rejection thereof on formal grounds. A marked up version the amended claim is attached hereto pursuant to 37 C.F.R. § 1.121(c)(ii). No new matter is involved. It is not Applicants' intent to surrender any equivalents based on the amendments and arguments presented herein.

In paragraph 2 on page 2 of the Office Action, claim 6 is rejected on formal grounds, as is claim 7 which depends upon claim 6. According to the Office Action, there is insufficient antecedent basis for the references to "400th", "320th" and "256th" in claim 6. Rather than change the dependency of claim 6 to claim 5 which refers to numbers of pixels and not data items, as such, Applicants are changing "the" to -- a -- in various places throughout claim 6 so as to properly introduce the limitations which follow. Therefore, claim 6 should now be clear and definite, as should be claim 7, which depends from claim 6.

In paragraph 4 which begins on page 2 of the Office Action, claims 1, 2, 8 and 10 are rejected under 35 U.S.C. § 102(a) as being anticipated by U.S. Patent 4,985,698 of Mano et al. Mano is said to teach all of the limitations of the claims. In paragraph 6 on page 4 of the Office Action, claim 5 is rejected under 35 U.S.C. § 102(a) as being anticipated by Mano et al. Again, Mano et al. is said to teach all of the limitations of claim 5. In paragraph 7 which begins on page 4 of the Office Action, claims 3, 4, 9, 11 and 19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Mano in view of U.S. Patent 5,977,944 of Kubota. Mano et al. is said to teach all of the limitations of the claims except for input-side and output-side line memory being small end-stage shift registers, and an input data switching circuit for switch output transferred data. For this, Kubota et al. is relied on.

In paragraph 8 on page 6 of the Office Action, claim 12 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Mano et al. in view of Kubota et al. and further in view of U.S. Patent 6,020,871 of Asada. Asada is relied upon for its

teaching or suggestion of the output-side memory further including a bi-directional shift register.

These rejections are respectfully traversed for the reasons discussed hereafter.

In paragraph 8 on page 6 of the Office Action, claims 13-18 are indicated as being allowable if rewritten in independent form.

Regarding the rejection of claims based on Mano et al., such reference has been carefully studied by Applicants. In claims 1 and 10 of the present invention, which are rejected on this reference, each of a plurality of memory portions for storing digital data assigned by a data separation portion includes an "input-side line memory" and an "output-side line memory". The input-side line memory stores the digital data assigned by the data separation portion and transfers in parallel the digital data to the corresponding output-side line memory. The output-side line memory holds the transfer data and has a plurality of output portions capable of serially outputting the held data from prescribed positions different from each other. One of the plurality of output portions of the output-side line memory is selected based on the number of pixels in the horizontal direction in the display section and analogy display data is output from the selected output portions to the display section.

In claim 1, for example, the signal processing circuit includes "a data separation portion for performing assignment of said input digital video data". Memory portions for storing the assigned digital data include "an input-side line memory having a data storage capacity equaled to or greater than the number of pixels of said display unit in a horizontal direction divided by the number of said regions and sequentially receiving and storing said digital data". It is also "an output-side line memory for holding the serial data stored in said input-side line memory and transferred in parallel from said input-side line memory and having a plurality of output portions capable of serially outputting the data held therein from

prescribed positions different from each other." As further defined in claim 1, "selection is made among said plurality of output portions of said output-side line memory in accordance with the number of pixels of said display unit in a horizontal direction", and "serial output data is supplied from the selected output portion in each of said plurality of memory portions to said display unit as analog displayed data".

In Mano et al., on the other hand, a horizontal driver is divided into N-sections (XDVL, XDVR), and N line memories (3, 4) are provided corresponding to the N divided sections. Each of the N line memories stores pixel data assigned by and supplied from a first MPX 2 and outputs the stored data to a second MPX 5. In other words, Mano et al. describes that input of data and output of data to the subsequent components are performed using a single line memory. There is no description or suggestion of having an input-side line memory and an output-side line memory as in each of the plurality of memory portions of the present invention. That is, there is no description or suggestion of separation of the reception function of data and the output function of data to the subsequent components as claimed in the present invention.

As noted above, in the case of the present invention, a memory portion includes an input-side line memory and an output-side line memory and, in particular, a plurality of output portions capable of serially outputting data from prescribed positions different from each other are provided in the output-side line memory so that data can be output from a desired output portion. With such a structure, it is possible to select an appropriate output portion corresponding to the number of pixels in the display section of a display device, and, consequently, it is possible to easily produce various display data suitable for various display devices having different numbers of pixels using a signal processor circuit having the same structure as described in the present invention. In this connection, please see the "Summary of the Invention" which begins on page 7 of the specification.

In Mano et al., line memories 3 and 4 having a storage capacity corresponding not only to the number of divisions of a horizontal driver, but also to the number of pixels to be driven by each horizontal driver must be selected, and therefore line memories 3 and 4 having different capacity must be provided for display devices having different numbers of pixels.

Moreover, by separately configuring the data reception function and data output function to the subsequent components within the input-side line memory and the output-side line memory, respectively, it is possible to facilitate processes such as a change in the order of data output from the order of data input by changing the order of selection of the output portions of the output-side line memory, as defined in, for example, in claim 14. In claim 14, "data is read out from said output-side memory in the reverse order from which data is input to said input side memory". Again, this is described in "Summary of the Invention" which begins on page 7 of the specification. In Mano et al., such processes cannot be performed.

Consequently, claims 1, 2, 5, 8 and 10 patentably distinguish over Mano et al.

Regarding the rejection of claims 3, 4, 9, 11, 12 and 19 on combinations of Mano et al. with other differences, such claims depend, directly or indirectly, from claim 1. As described above, claim 1 is clearly distinguishable from Mano et al., consequently, claims 3, 4, 9, 11, 12 and 19 are submitted to clearly distinguish patentably over the attempted combination of references for at least the same reasons.

Regarding Kubota, while such reference discloses a display device in which a data output circuit divided into a plurality of blocks comprises a shift register, such reference fails to disclose or even suggest that each of a plurality of memory portions comprises and input-side line memory and an output-side line memory, as in the case of the present invention. Consequently, the present invention cannot be achieved, even if the combination of Mano and Kubota is attempted.

In conclusion, claims 1-12 and 19 are submitted to clearly distinguish patentably over the prior art, for the reasons discussed above, in addition to claims 13-18. Claim 6 as amended is clear and definite, as also previously described. Therefore, reconsideration and allowance of the application, as amended, are respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles telephone number (213) 337-6742 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,

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Version with markings to show changes made:

6. (Amended) The signal processing circuit recited in claim 1, wherein said plurality of output portions of said output-side line memory can output serial data in a sequential manner starting from [the] a 400th, a 320th, and a 256th data [items] item counting from [the] a last input data item of said digital data serially input to said input-side line memory.